Claims

[c1] 1. An oscillator delay stage circuit operating between first and second operating voltages, wherein the first operating voltage is higher than the second operating voltage, the oscillator delay stage circuit comprising:
(a) an inverting circuit including an input node and an output node,
wherein the inverting circuit is configured to receive an input signal from the input node and generate an output signal to the output node, and
wherein the inverting circuit is further configured to increase the output signal in voltage in response to the input signal decreasing in voltage and to decrease the output signal in voltage in response to the input signal increasing in voltage; and
(b) a control circuit including a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the second operating voltage,
wherein in response to the input signal increasing in voltage towards the first operating voltage, the first switch circuit is configured to decrease in resistance, and
wherein the first resistance adjusting circuit is config-

ured to receive as input an external control signal and to change in resistance in response to a change of the external control signal.

[c2] 2. The oscillator delay stage circuit of claim 1, wherein the first switch circuit comprises a transistor having a gate terminal configured to receive the input signal.

[c3] 3. The oscillator delay stage circuit of claim 2, wherein the transistor is an n-channel transistor.

[c4] 4. The oscillator delay stage circuit of claim 1, wherein the first resistance adjusting circuit comprises a transistor having a gate terminal configured to receive the external control signal.

[c5] 5. The oscillator delay stage circuit of claim 4, wherein the transistor is an n-channel transistor.

[c6] 6. The oscillator delay stage circuit of claim 1, wherein the inverting circuit comprises a CMOS inverter.

[c7] 7. The oscillator delay stage circuit of claim 1, wherein the control circuit further comprises an extrinsic capacitor electrically coupled between the output node and the second operating voltage.

[c8] 8. The oscillator delay stage circuit of claim 1, wherein the inverting circuit further comprises a second switch

circuit and a second resistance adjusting circuit electrically coupled in series between the output node and the first operating voltage,
wherein in response to the input signal decreasing in voltage towards the second operating voltage, the second switch circuit is configured to decrease in resistance, and
wherein the second resistance adjusting circuit is configured to receive as input the external control signal and to change in resistance in response to the change of the external control signal.

[c9] 9. An oscillator delay stage circuit operating between first and second operating voltages, wherein the first operating voltage is higher than the second operating voltage, the oscillator delay stage circuit comprising:
(a) an inverting circuit including an input node and an output node,
wherein the inverting circuit is configured to receive an input signal from the input node and generate an output signal to the output node, and
wherein the inverting circuit is further configured to increase the output signal in voltage in response to the input signal decreasing in voltage and to decrease the output signal in voltage in response to the input signal increasing in voltage; and

(b) a control circuit including a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the first operating voltage,

wherein in response to the input signal decreasing in voltage towards the second operating voltage, the first switch circuit is configured to decrease in resistance, and wherein the first resistance adjusting circuit is configured to receive as input an external control signal and to change in resistance in response to a change of the external control signal.

[c10] 10. The oscillator delay stage circuit of claim 9, wherein the first switch circuit comprises a transistor having a gate terminal configured to receive the input signal.

[c11] 11. The oscillator delay stage circuit of claim 10, wherein the transistor is a p-channel transistor.

[c12] 12. The oscillator delay stage circuit of claim 9, wherein the first resistance adjusting circuit comprises a transistor having a gate terminal configured to receive the external control signal.

[c13] 13. The oscillator delay stage circuit of claim 12, wherein the transistor is an n-channel transistor.

[c14] 14. The oscillator delay stage circuit of claim 9, wherein

the inverting circuit comprises a CMOS inverter.

[c15] 15. The oscillator delay stage circuit of claim 9, wherein the control circuit further comprises an extrinsic capacitor electrically coupled between the output node and the first operating voltage.

[c16] 16. The oscillator delay stage circuit of claim 9, wherein the inverting circuit further comprises a second switch circuit and a second resistance adjusting circuit electrically coupled in series between the output node and the second operating voltage,
wherein in response to the input signal increasing in voltage towards the first operating voltage, the second switch circuit is configured to decrease in resistance, and wherein the second resistance adjusting circuit is configured to receive as input the external control signal and to change in resistance in response to the change of the external control signal.

[c17] 17. A method for signal generation, the method comprising the steps of:
(a) providing a voltage-controlled oscillator comprising N oscillator delay stage circuits operating between first and second operating voltages, N being an odd integer, the first operating voltage being higher than the second operating voltage, wherein each of the N oscillator delay

stage circuits comprises:

(i) an inverting circuit including an input node and an output node, and

(ii) a control circuit including a switch circuit and a resistance adjusting circuit electrically coupled in series between the output node and the second operating voltage;

(b) applying to the resistance adjusting circuit an external control signal so as to achieve a target operating frequency for the voltage-controlled oscillator;

(c) in response to an input signal rising in voltage at the input node,

(i) using the inverting circuit to decrease an output signal in voltage at the output node, and

(ii) decreasing the resistance of the switch circuit.

[c18] 18. The method of claim 17, wherein the switch circuit comprises a transistor having a gate terminal configured to receive the input signal.

[c19] 19. The method of claim 17, wherein the resistance adjusting circuit comprises a transistor having a gate terminal configured to receive the external control signal.

[c20] 20. The method of claim 17, wherein the inverting circuit comprises a CMOS inverter.